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Review on thermal challenges in embedded system

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Abstract

Embedded systems are used in safety critical areas such as automotive electronics and medical applications. These safety critical applications impose strict requirements on reliability, performance, low power and testability of the underlying VLSI circuits. The VLSI circuits operate very often at high temperature, which has negative impact on reliability, performance, power-efficiency and testability with silicon technology scaling. Several thermal impacts on VLSI circuits and their related challenges are discussed. This paper presents also a few emerging techniques that take temperature into account in the design and test processes. There are number of embedded computers controlling virtually all devices and systems in a huge spectrum of application areas including aerospace, manufacturing, chemical processes, healthcare care, automotive, transportation, telecommunication, and consumer appliances. Many of these systems are safety-critical, such as automotive electronics and medical equipment, with stringent reliability and real time requirements. At the same time, with silicon technology scaling, VLSI circuits used to implement the computational components of these systems are built with smaller transistors, operate at higher clock frequency, run at lower voltage levels, and operate very often at higher temperature. Consequently, they are subject to more faults and interferences.

Keywords-*Dynamic Thermal Management; Burn-in; Principal Orthogonal Decomposition; Model-Based Design*

1.INTRODUCTION

Recently embedded system encountered many constraints such as power, energy, reliability, and temperature. Among these challenging issues, temperature related issues have become especially important within the past several years. This paper summarizes recent thermal management techniques for embedded system. Temperature monitoring, requirement for Dynamic Thermal Management (DTM), includes temperature estimation and sensor placement techniques for accurate temperature measurement or estimation. Micro architectural techniques include both static and dynamic thermal management techniques that control hardware structures. Floor planning covers a range of thermal-aware floor planning techniques for 2D and 3D microprocessors. OS/ compiler techniques include thermal-aware task scheduling and instruction scheduling techniques. Liquid cooling techniques are higher capacity alternatives to conventional air cooling techniques. Thermal reliability/security issues cover temperature-dependent reliability modeling, Dynamic Reliability Management (DRM), and malicious codes that specifically cause overheating. Temperature-related issues will only become more challenging as process technology continues to evolve and transistor densities scale up faster than power per transistor scales down.

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I.1 Three Modes of Heat Transfer

A. Conduction

Thermal conduction is the process in which thermal energy transfers through matter, from a region of higher temperature to lower temperature and acts to equalize the temperature difference. It can also be described as the heat energy transferred from one material to another by direct contact. Fourier's Law of Conduction states that the rate of heat flow equals the product of the area normal to the heat flow path, the temperature gradient along the path and the thermal conductivity of the medium. Heat flux, "q" is the rate of heat transfer per unit area and it depends on the direction. Consider a one dimensional block with one side at a constant T1 and the others

B. Convection

Convection is the transfer of thermal energy between two surfaces as a consequence of a relative velocity between them. The most practical application is where one surface is a solid and the other is a fluid.ide at a constant T2, where T1 > T2. On a basic level, the convective heat transfer can be improved with higher airflow and more surface area. However, it is not always possible to make the thermal solution larger or increase the airflow, due the constraints of embedded form factors. Therefore, the thermal solution designer must factor in all the boundary conditions in order to develop a suitable solution. Convective heat transfer plays a very important role in electronics cooling. This mode of heat transfer will allow higher power processors to be cooled in most applications.

C. Radiation

Radiation cooling is the transfer of heat by electromagnetic emission, primarily in the infrared wavelengths. While the transfer of energy by conduction and convection requires the presence of a material medium, radiation does not. In fact, radiation transfer occurs most effectively in a vacuum. Graphically represents the radiation heat transfer between two surfaces at different temperatures. For the majority of embedded applications, radiation will result in a very small percentage of the total heat transfer. The only applications where it will have significant impact are in fan less designs.

2. LITERATURE SURVEY

Oleg Semenov et al (2003) presented burn-in which is performed at elevated temperature, which is achieved by special equipment .This approach will not be able to achieve the specified temperature gradients, especially those with large magnitudes. Burn-in is a quality improvement procedure challenged by the high leakage currents that are rapidly increasing with IC technology scaling. These currents are expected to increase even more under the new burn-in environments leading to higher junction temperatures, possible thermal runaway, and yield loss during burn-in. It can be estimate the increase in junction temperature with technology scaling. It shows that under normal operating conditions, the junction temperature is increasing 1.45 /generation. The increase in junction temperature under the burn-in condition was found to be exponential. The range of optimal burn-in voltage and temperature is reduced significantly with technology scaling.

Dettori M et al (2003) formulated the principal Orthogonal decomposition (POD) used to develop a low-order nonlinear model which simulation results for tracking a ramp with rate 50 C/sec with a controller scheme that includes feedback, feed forward and pre filter and investigates the application of model-based control design techniques to distributed temperature control systems. Multivariable controllers are an essential part of the modern-day rapid thermal processing (RTP) systems. This paper considers all aspects of the control problem beginning with a physics-based model and concluding with implementation of the real-time embedded controller. The thermal system used as an example throughout the paper is a RTP chamber that is widely used in semiconductor wafer processing. With its exceptionally stringent performance requirements of wafer temperature, high temperature ramp rates, RTP temperature control is a challenging distributed temperature control problem. Additionally, it is an important problem in the semiconductor industry because of the progressively smaller "thermal budget" resulting from ever decreasing integrated circuit dimensions.

Jon L. E et al (2003)formulated model-based control system design which has excellent temperature control on both the low-order and the full nonlinear simulations and need for addition of run-to-run control to deal with system nonlinearities. Model-Based Design (MBD) is a mathematical and visual method of addressing problems associated with designing complex control, signal processing and communication systems. It is used in many motion controls, industrial equipment, aerospace, and automotive applications. Model-based design is a methodology applied in designing embedded software. MBD provides an efficient approach for establishing a common framework for communication throughout the design process while supporting the development cycle . In model-based design of control systems, development is manifested in these four steps: 1) modeling a plant, 2) analyzing and synthesizing a controller for the plant, 3) simulating the plant and controller, and 4) integrating all these phases by deploying the controller.

Jayanth Srinivasan et al (2004) formulated RAMP industrial strength model which has high correlation between application power and temperature. The relentless scaling of CMOS technology has provided a steady increase in processor performance for the past three decades. However, increased power densities and other scaling effects have an adverse impact on long term processor lifetime reliability. This paper represents a first attempt at quantifying the impact of scaling on lifetime reliability due to intrinsic hard errors, taking workload characteristics into consideration. For our quantitative evaluation, we use RAMP previously proposed industrial strength model that provides reliability estimates for a workload, but for a given technology.

Chen F et al(2004) has developed the methodology of effective thermal conductivity which allows quick evaluation of various Cullow-k campasite interconnect structures advancement in thermal properties of low-k dielectrics and better chip cooling designs could be critical to future technologies. Demonstrated that interconnect Joule heating and low thermal conductivity of low-k dielectric materials can have a large impact on chip reliability and performance.

Liao w et al (2006) formulated genetic algorithm to solve problems with multiple solutions. The advantage is that it solves problems with multiple solutions but it cannot assure constant optimization response times. The value of average current becomes stable when the circuit is in the computer science field of. This heuristic (also so artificial intelligence, a genetic algorithm is a search heuristic that mimics the process of natural selection sometimes called a meta heuristic) is routinely used to generate useful solutions to optimization and search problems. Genetic algorithms belong to the larger class of evolutionary algorithms(EA), which generate solutions to optimization problems using techniques inspired by natural evolution, such as inheritance, mutation, selection, and crossover. Genetic algorithms find application in bioinformatics, phylogenetics, computational science, engineering, economics, chemistry, manufacturing, mathematics, physics, pharma cometrics and other fields.

Lio.Y et al (2007) presented thermal-constrained energy optimization procedure to minimize system energy consumption under a constraint on peak temperature which optimizes energy under a constraint on peak temperature. If the bound is too loose, the system may operate at an unnecessary-high temperature average which results in 11 °C temperature reduction with 8.3% energy overhead are designed using the small cell library.

.Flament et al (2009) formulated ALARA (As Low As Reasonably Achievable)low as reasonably practicable. IC modeling using fault injection and simulation techniques could be performed to evaluate mitigation efficiency. The implementation of equipments with embedded electronic to monitor, control, measure and operate future large facilities dedicated to high energy physics or nuclear fusion are necessary. Reliable operation of these equipments will be achieved through availability and reliability analysis. In several cases, the equipment selection or development approach has to be done by considering a harsh environment in terms of radiations. In order to implement these systems in such environments shielding, location and distance from the source must be considered to reduce, to protect and to avoid radiation effects. People in charge of the choice of the equipments have to take into account and mitigate radiation effects from subsystem to system level. This requires an approach integrating tradeoff between performance and reliability, between the use of the state of the art of technologies and robust and well known devices. Experience and knowledge from previous programs should be considered to build approach and strategy that may be necessary to overcome difficulties. In the present paper, we will review the main challenges faced by designers for systems implementation with embedded electronics in future facilities dedicated to international physics programs.

Zebo Peng et al (2010) time-redundancy based fault-tolerance techniques handle transient faults and the hardware/ software trade-offs related to fault detection and fault tolerance with the increased silicon area, additional design effort, lower production quantities, excessive power consumption, and protection mechanisms against radiation (such as shields). It deals with the design of embedded systems for safety-critical applications,

where both fault tolerance and real-time requirements should be taken into account at the same time. With silicon technology scaling, integrated circuits are implemented with smaller transistors, operate at higher clock frequency, and run at lower voltage levels. As a result, they are subject to more faults, in particular, transient faults. Additionally, in nano-scale technology, physics-based random variations play an important role in many device performance metrics, and have led to many new defects. It describes several key challenges and presents several emerging solutions to the design and optimization of such systems. In particular, it discusses the advantages of using time-redundancy based fault-tolerance techniques that are triggered by fault occurrences to handle transient faults and the hardware/ software trade-offs related to fault detection and fault tolerance.

Nima Aghaee et al (2014) formulated an algorithm such as Burn in which has an advantage such as low cost in a reasonably short time and the disadvantage is that it do not sufficiently speed up the formation of the defects that depend on large temperature gradients and consequently such early-life defects will go undetected. Burn-in is usually carried out with high temperature and elevated voltage. Since some of the early-life failures depend not only on high temperature but also on temperature gradients, simply rising up the temperature of an IC is not sufficient to detect them. This is especially true for 3D stacked ICs, since they have usually very large temperature gradients. The efficient detection of these early-life failures requires that specific temperature gradients are enforced as a part of the burn-in process. This paper presents an efficient method to do so by applying high power stimuli to the cores of the IC under burn-in through the test access mechanism. Therefore, no external heating equipment is required. The scheduling of the heating and cooling intervals to achieve the required temperature gradients is based on thermal simulations and is guided by functions derived from a set of thermal equations.

Peng.z et al (2014) formulated electro migration and time-dependent dielectric breakdown which is efficient but Time consuming which results in amplitude and frequency of temperature oscillation has a huge impact on the overall lifetime of a chip. More and more embedded systems are used in safety-critical areas such as automotive electronics and medical applications. These safety critical applications impose stringent requirements on reliability, performance, low power and testability of the underlying VLSI circuits. With silicon technology scaling, VLSI circuits operate very often at high temperature, which has negative impact on reliability, performance, power-efficiency and testability. This paper discusses several thermal impacts on VLSI circuits and their related challenges. It presents few emerging techniques that take temperature into account in the design and testprocesses

3. COMPARATIVE ANALYSIS

TABLE 1.COMPARATIVE ANALYSIS

Author	Year	Algorithm	Advantages	Disadvantages	Results
Peng.z et al	2014	.electro-migration and time-dependent dielectric breakdown	efficient	Time consuming	Amplitude & frequency scillation— has huge impact on the overall lifetime
Nima	2014	Burn in	low cost in a reasonably short time	does not sufficiently speed up the formation of the defects that depend on large temperature gradients and consequently such early-life defects will go undetected.	
Aghaee et al					
Zebo Peng et al	2010	time-redundancy based fault-tolerance techniques	handle transient faults and hardware/software trade-offs related to fault detection and fault tolerance	increased silicon area, lower production quantities, excessive power consumption, & protection mechanisms against radiation	
Lio.y et al	2007	thermal-constrained energy optimization procedure to minimize system.	optimize energy under a constraint on peak temperature.	If the bound is too loose, the system may operate at an unnecessary-high temperature	average 11 °C temperature reduction with 8.3% energy overhead
Weiping	2006	Genetic algorithm	It solves problems with multiple solutions.	cannot assure constant optimisation response times.	The value of average current become stable when the circuits are designed
Liao et al					
Jayanth	2004	RAMP [industrial stenght model]			High correlation between application power and temperature
Srinivasan et al					
F. Chen et al	2004	effective thermal conductivity	allows quick evaluation of various Cullow-k campasite interwnnect structures	advancement in thermal properties of low-k dielectrics and better chip cooling designs could be critical to future technologies.	interconnect Joule heating and low thermal conductivity of low-k dielectric materials can have a large impact on chip reliability and performance
Oleg	2003		performed at elevated temperature, which is achieved by special equipment	not able to achieve the specified temperature gradients, especially those with large magnitudes.	
Semenov et al		burn-in			
Dettori.m et al	2003	1.principal Orthogonal decomposition (POD)	used to develop a low-order nonlinear model.	.	simulation results for tracking ramp with rate 50 C/sec scheme that includes feedback, feedforward
Jon L. E et al	2003	model-based control system design	excellent temperature control on both the low-order and the full nonlinear simulations.	need for addition of run-to-run control to deal with system nonlinearities	

4. CONCLUSION

Embedded systems for safety-critical applications have put stringent requirements on reliability, performance, power-efficiency and testability of the underlying VLSI circuits. These different requirements are all impacted by the temperature the chip. This survey paper has discussed several of these thermal impacts and their related challenges. It has also presented briefly several emerging techniques that take temperature into account in the design and test processes of embedded systems, especially at the system level. The issues are discussed in this paper such as the influence of temperature on reliability, power consumption, and testability, are not new, taken individually. However, the interplay of these issues and their increased impacts has led to many great challenges. In particular, there are still many open problems in how to develop efficient global optimization techniques to consider the different thermal impacts and other design requirements at the same time, so that it can build highly reliable and predictable embedded systems in an efficient manner. This paper provides an overview of the reliability modeling for embedded system and a perspective of the different system level design techniques for lifetime optimization.

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